AMENDMENT

Amendments to the Specification

Please replace the full paragraph beginning on line 24 of page 8 with the following paragraph:

[0040] The processor task engine 100 also includes a task control unit 106 that communicates with the task queue 104 through a task controller bus 103. The task control unit 106 includes an instruction decoder 108 that decompresses and decodes the instructions stored in an instruction memory so that they can be understood and executed by the task engine 100. The task control unit 106 also includes a branch control unit 110 that controls the order of executing instructions in the processor task engine ~~110~~100.

Please replace the full paragraph beginning on line 13 of page 11 with the following paragraph:

[0052] An instruction decoder 154 decodes the decompressed instructions to generate instructions that can be executed by the computational or logic units 124. The branch control unit 110 controls the order of executing instructions in the processor task engine 110. The task controller unit 106 also includes constant registers 156.

Please replace the full paragraph beginning on line 6 of page 14 with the following paragraph:

[0064] Fig. 6c illustrates another embodiment of a programmable multi-processor system architecture 2210 that includes a plurality of VLIW processor task engines 100 according to the present invention. The multi-processor system architecture 210 includes three processor task engines 100. Each of the processor task engines 100 is coupled to the Q-bus 102. The multi-processor system architecture 210 also includes two I/O units 202 that input data to the multi-processor system 210 and that output resulting or computed data. The I/O units 202 are coupled

to the Q-bus and coupled to one of the VLIW processor task engines 100.

Please replace the full paragraph beginning on line 5 of page 19 with the following paragraph:

[0086] The designer configurable task engines and the multi-processor systems of the present invention are well suited for System on Chip (SoC) architectures and have numerous advantages over prior art custom integrated circuits. The designer configurable task engines offer high-performance with a high degree of programmability. These task engines and systems providing a high-level of parallelism and the ability to define custom data path elements. These features eliminate the need for custom logic blocks, which reduces the total cost of the system and increases the time to market.